



# STB11NB40 STB11NB40-1

N-CHANNEL 400V - 0.48  $\Omega$  - 10.7A D<sup>2</sup>PAK/I<sup>2</sup>PAK  
PowerMESH™ MOSFET

**Table 1. General Features**

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB11NB40	400 V	< 0.55 $\Omega$	10.7 A
STB11NB40-1	400 V	< 0.55 $\Omega$	10.7 A

### FEATURES SUMMARY

- TYPICAL R<sub>DS(on)</sub> = 0.48  $\Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

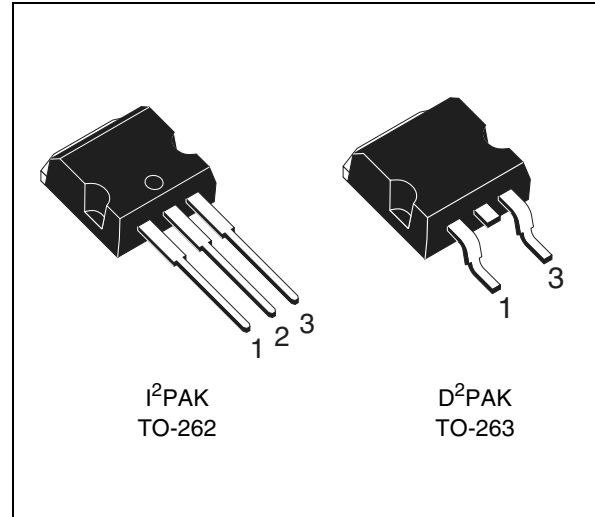
### DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R<sub>DS(on)</sub> per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

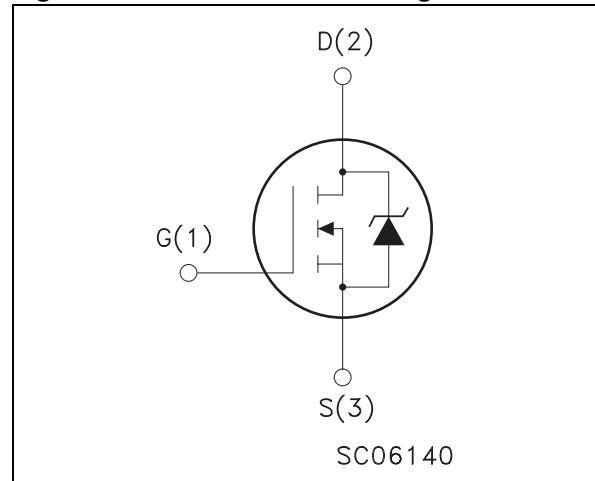
### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

**Figure 1. Package**



**Figure 2. Internal Schematic Diagram**



**Table 2. Order Codes**

Part Number	Marking	Package	Packaging
STB11NB40T4	B11NB40	D <sup>2</sup> PAK	TAPE & REEL
STB11NB40-1	B11NB40	I <sup>2</sup> PAK	TUBE

## STB11NB40/STB11NB40-1

**Table 3. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	400	V
$V_{DGR}$	Drain- gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	400	V
$V_{GS}$	Gate-source Voltage	$\pm 30$	V
$I_D$	Drain Current (cont.) at $T_C = 25\text{ }^\circ\text{C}$	10.7	A
$I_D$	Drain Current (cont.) at $T_C = 100\text{ }^\circ\text{C}$	6.7	A
$I_{DM}^{(1)}$	Drain Current (pulsed)	42.8	A
$P_{tot}$	Total Dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
	Derating Factor	1.0	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Storage Temperature	4.5	V/ns
$T_{stg}$	Storage Temperature	-65 to 150	$^\circ\text{C}$
$T_j$	Max. Operating Junction Temperature	150	$^\circ\text{C}$

Note: 1. Pulse width limited by safe operating area  
2.  $I_{SD} \leq 11\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$

**Table 4. Thermal Data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-case Max	1.0	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

**Table 5. Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max, $\delta < 1\%$ )	10.7	A
EAS	Single Pulse Avalanche Energy (starting $T_j = 25\text{ }^\circ\text{C}$ ; $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ )	530	mJ

**ELECTRICAL CHARACTERISTICS** ( $T_{\text{case}} = 25^{\circ}\text{C}$  unless otherwise specified)**Table 6. Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source Breakdown Voltage	$I_{\text{D}} = 250 \mu\text{A}; V_{\text{GS}} = 0$	400			V
$I_{\text{DSS}}$	Zero Gate Voltage	$V_{\text{DS}} = \text{Max Rating}$			1	$\mu\text{A}$
	Drain Current ( $V_{\text{GS}} = 0$ )	$V_{\text{DS}} = \text{Max Rating } T_{\text{c}} = 125^{\circ}\text{C}$			50	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-body Leakage Current ( $V_{\text{DS}} = 0$ )	$V_{\text{GS}} = \pm 30 \text{ V}$			$\pm 100$	nA

**Table 7. On** <sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}; I_{\text{D}} = 250 \mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static Drain-source On Resistance	$V_{\text{GS}} = 10\text{V}; I_{\text{D}} = 5.3 \text{ A}$		0.48	0.55	$\Omega$

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %**Table 8. Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{\text{fs}}$ <sup>(1)</sup>	Forward Transconductance	$V_{\text{DS}} > I_{\text{D(on)}} \times R_{\text{DS(on)max}}; I_{\text{D}} = 5.3 \text{ A}$	5	6.5		S
$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = 25 \text{ V}; f = 1 \text{ MHz}; V_{\text{GS}} = 0$		1115	1450	pF
$C_{\text{oss}}$	Output Capacitance			210	280	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance			22	30	pF

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %**Table 9. Switching On**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on Time	$V_{\text{DD}} = 200 \text{ V}; I_{\text{D}} = 5.3 \text{ A}; R_{\text{G}} = 4.7 \Omega$		17	25	ns
$t_{\text{r}}$	Rise Time	$V_{\text{GS}} = 10 \text{ V}$ (see test circuit, Figure 16)		10	15	ns
$Q_{\text{g}}$	Total Gate Charge	$V_{\text{DD}} = 320 \text{ V}; I_{\text{D}} = 10.7 \text{ A}; V_{\text{GS}} = 10 \text{ V}$		29.5	43	nC
$Q_{\text{gs}}$	Gate-Source Charge			10.6		nC
$Q_{\text{gd}}$	Gate-Drain Charge			11.8		nC

**Table 10. Switching Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{\text{r(Voff)}}$	Off-voltage Rise Time	$V_{\text{DD}} = 320 \text{ V}; I_{\text{D}} = 10.7 \text{ A}; R_{\text{G}} = 4.7 \Omega$ $V_{\text{GS}} = 10 \text{ V}$ ; (see test circuit, Figure 18)		10	14	ns
$t_{\text{f}}$	Fall Time			10	14	ns
$t_{\text{c}}$	Cross-over Time			17	25	ns

Table 11. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				10.7	A
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)				42.8	A
$V_{SD}^{(2)}$	Forward On Voltage	$I_{SD} = 10.7 \text{ A}; V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 10.7 \text{ A}; di/dt = 100 \text{ A}/\mu\text{s}$		400		ns
$Q_{rr}$	Reverse RecoveryCharge	$V_{DD} = 100 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$ (see test circuit, Figure 18)		3.4		$\mu\text{C}$
$I_{RRAM}$	Reverse RecoveryCharge			17		A

Note: 1. Pulse width limited by safe operating area  
 2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

Figure 3. Safe Operating Area

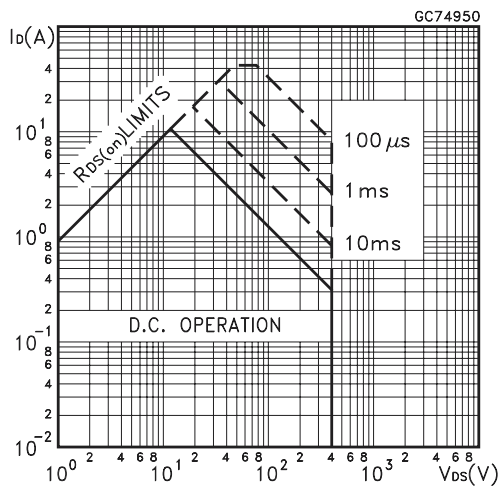


Figure 4. Thermal Impedance

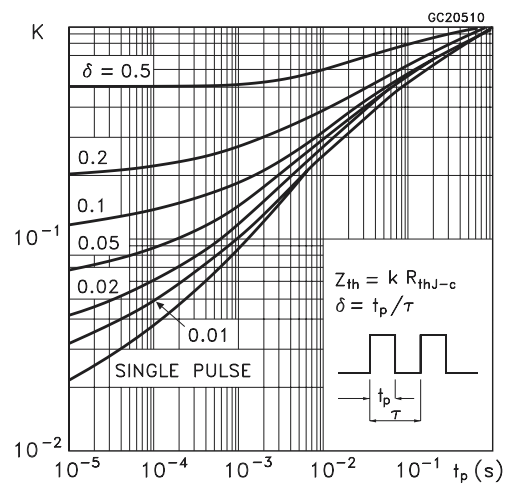


Figure 5. Output Characteristics

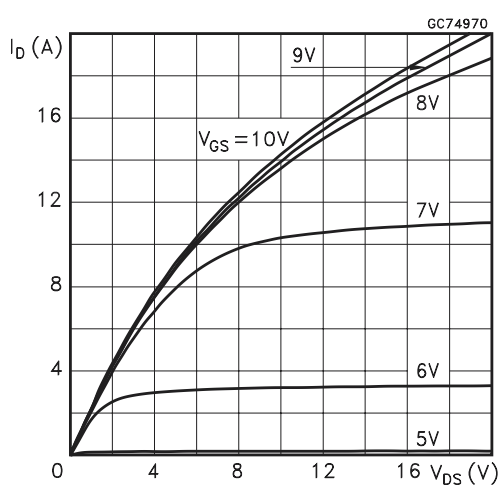


Figure 6. Transfer Characteristics

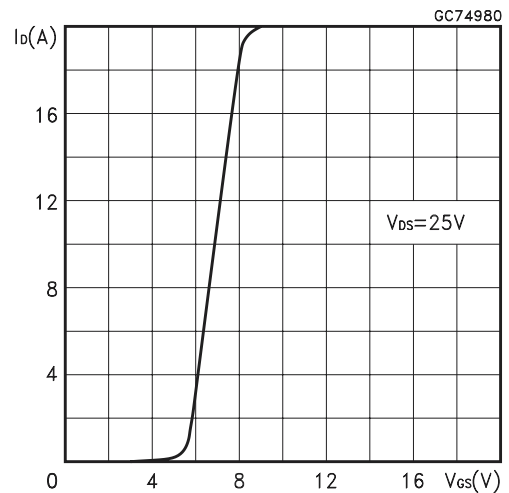


Figure 7. Transconductance

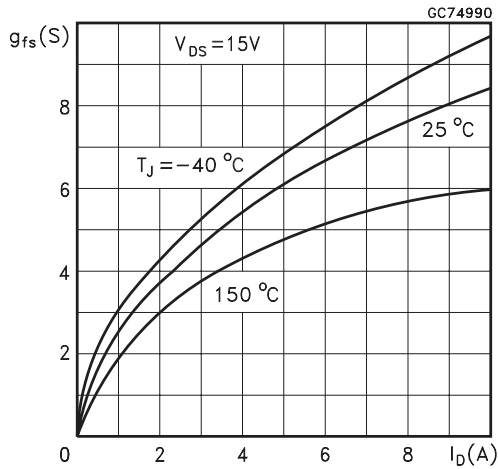


Figure 8. Static Drain-source On Resistance

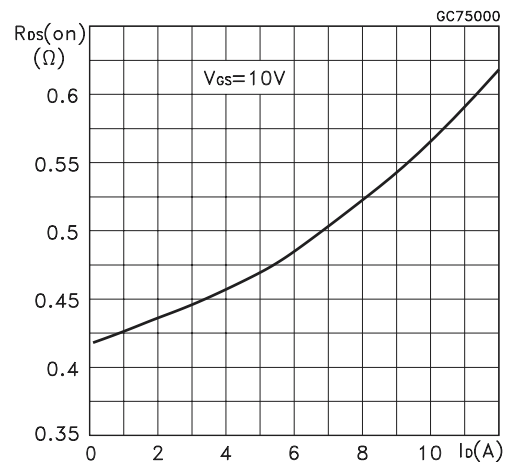


Figure 9. Gate Charge vs Gate-source Voltage

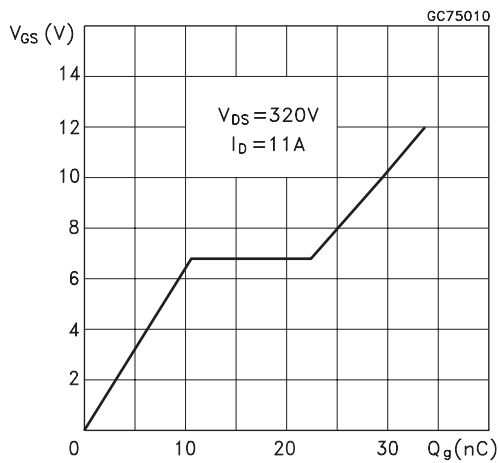


Figure 10. Capacitance Variations

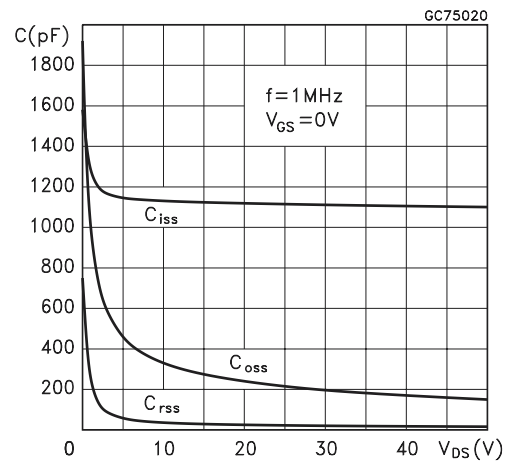


Figure 11. Normalized Gate Threshold Voltage vs Temperature

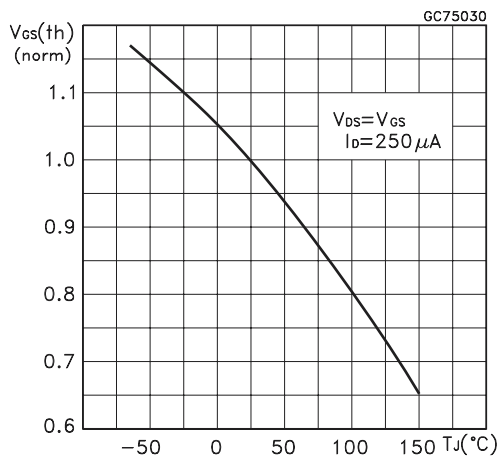
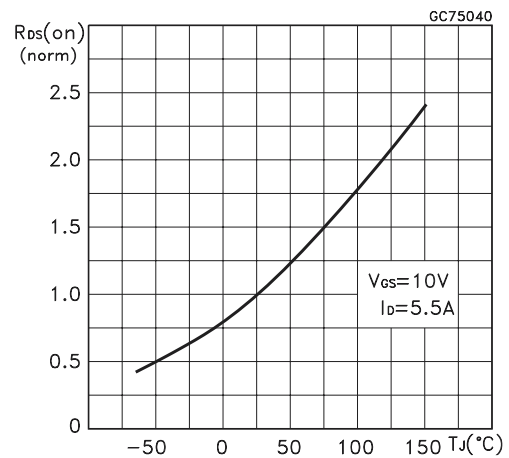
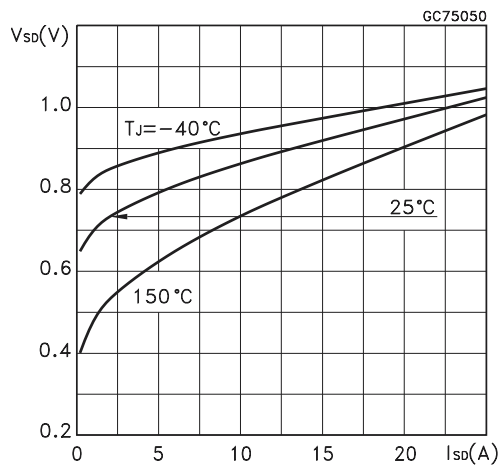


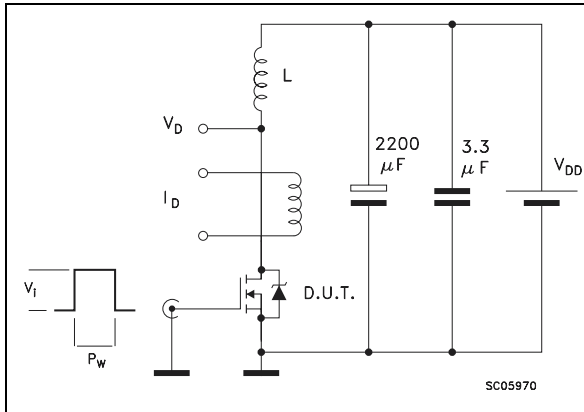
Figure 12. Normalized On Resistance vs Temperature



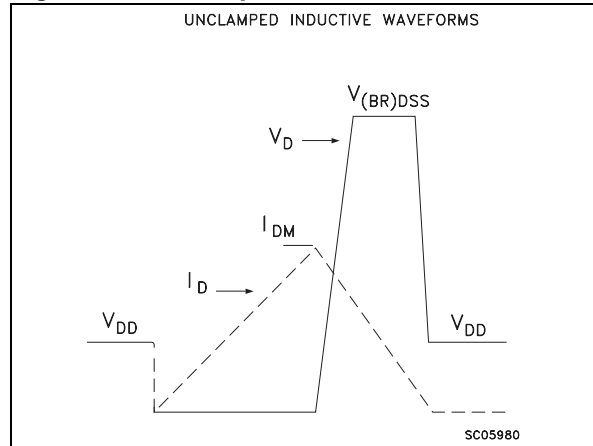
**Figure 13. Source-drain Diode Forward Characteristics**



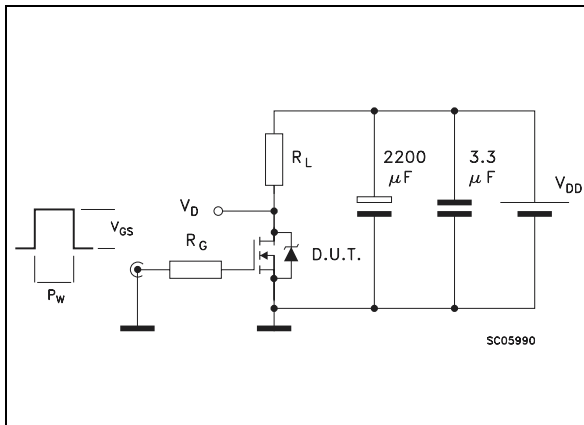
**Figure 14. Unclamped Inductive Load Test Circuit**



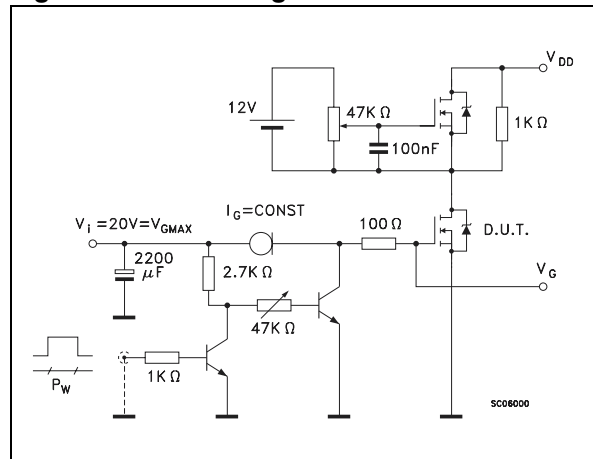
**Figure 15. Unclamped Inductive Waveforms**



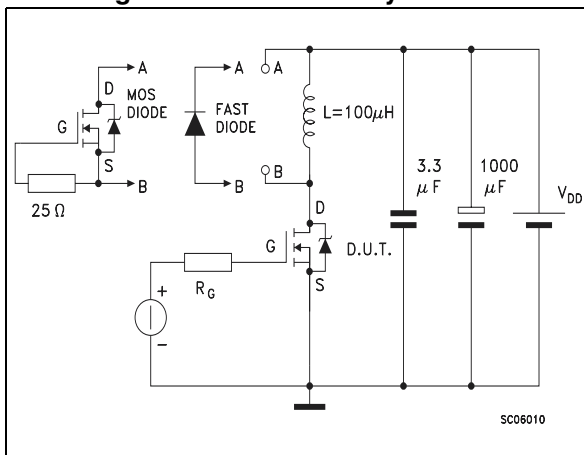
**Figure 16. Switching Times Test Circuits For Resistive Load**



**Figure 17. Gate Charge Test Circuit**



**Figure 18. Test Circuit For Inductive Load Switching And Diode Recovery Times**

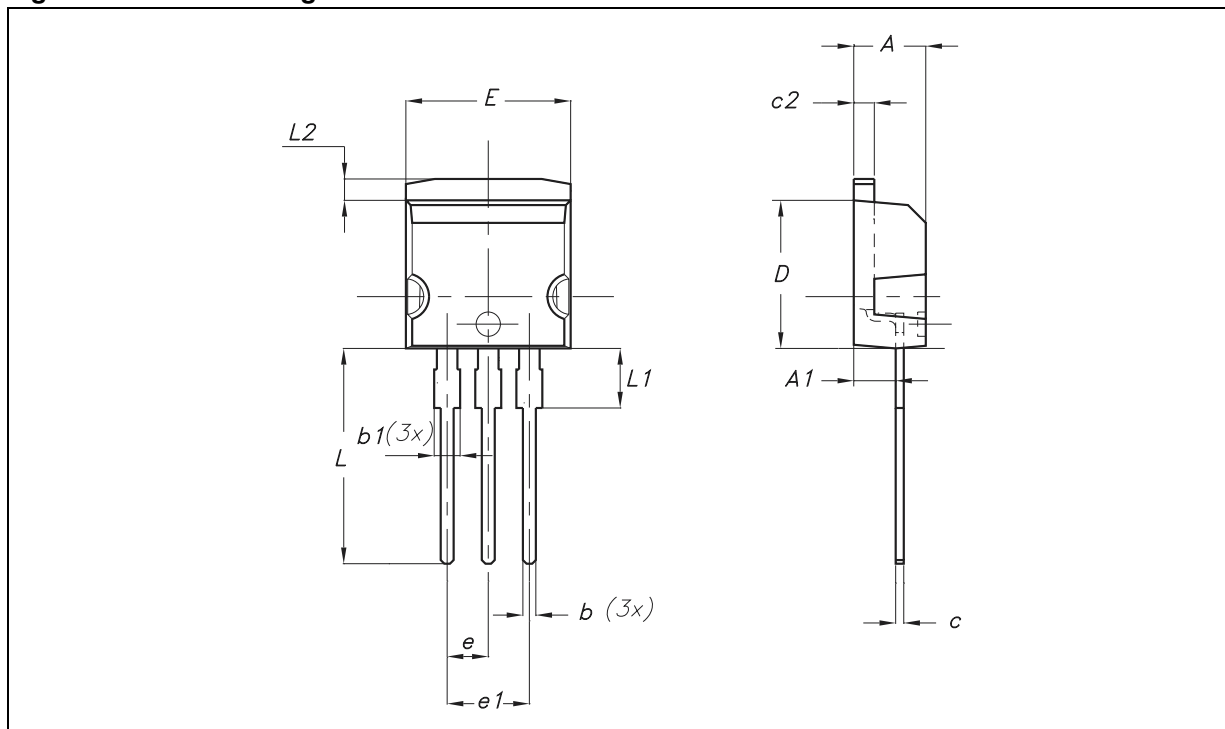


PACKAGE MECHANICAL

Table 12. I<sup>2</sup>PAK Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.349
b1	1.14		1.70	0.045		0.067
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.195		0.203
E	10.00		10.40	0.394		0.409
L	13.00		14.00	0.511		0.551
L1	3.50		3.93	0.138		0.154
L2	1.27		1.40	0.050		0.055

Figure 19. I<sup>2</sup>PAK Package Dimensions



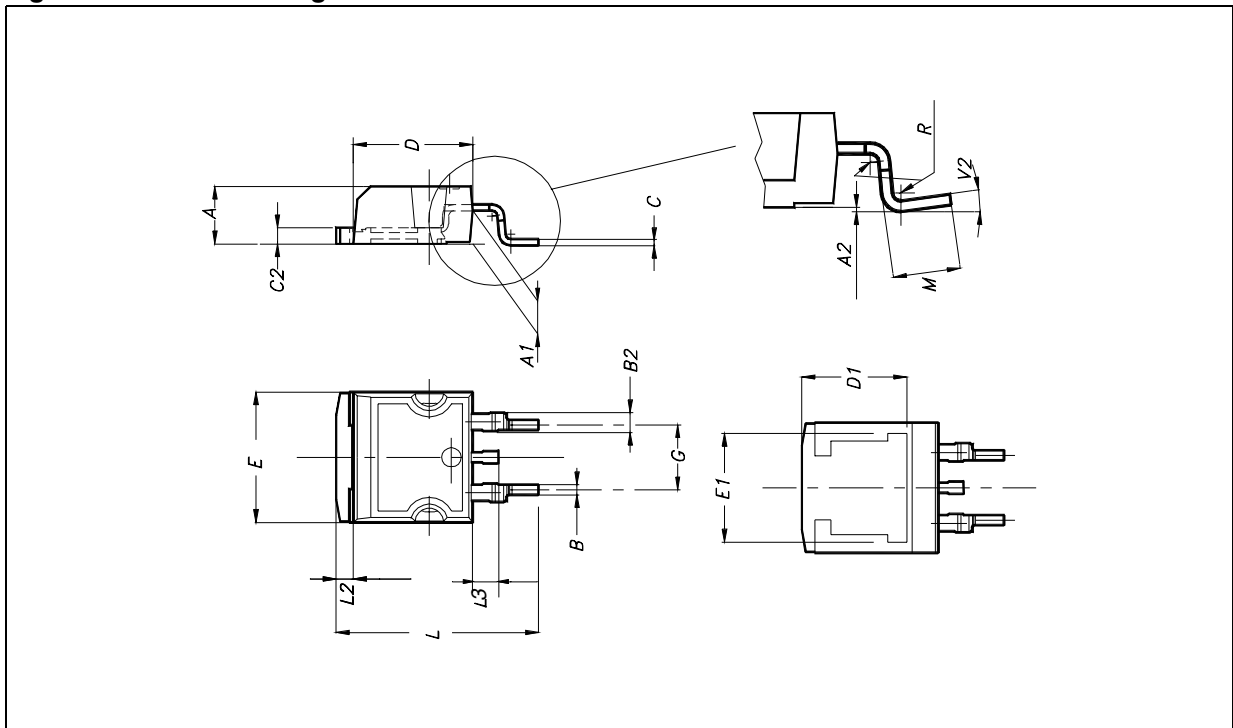
Note: Drawing is not to scale.



Table 13. D<sup>2</sup>PAK Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

Figure 20. D<sup>2</sup>PAK Package Dimensions



Note: Drawing is not to scale.

**REVISION HISTORY**

**Table 14. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
March-1998	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.

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